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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,537	09/10/2003	Kiyohiko Yamazaki	KAT 253	1951

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EXAMINER	
EJAZ, NAHEED	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,537	YAMAZAKI, KIYOHIKO	
	Examiner	Art Unit	
	Naheed Ejaz	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,8,11,12,16,17 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8,11,12,16,17 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments/Remarks

1. Applicant's arguments filed on 05/01/2006 have been fully considered but they are not persuasive.

2. Applicant argues: "To the extent that Hachisuka's switch 112 can be characterized as a mode selector, the modes that it selects are clearly either a digital reproduction mode or an FM analog reproduction mode. An ordinarily skilled person would have had no reason to think that Hachisuka's switch 12 selects either a reproduction mode of reproducing digital signals or "an evaluation mode of evaluating the digital signals" in accordance with claim 1". This is not persuasive. In the light of specification, evaluation mode is being selected to detect / evaluate error quantity (specification, paragraph # 0027) in the received signal before it gets to be decoded by ADPCM CODEC (figure 1, element 24a). Hachisuka is evaluating the signal by comparing it's noise component with specified value (could be responsible to generate an error in the received signal) and determines if the strength of the signal is not less then specified value which reads on claim limitations since evaluation mode is detecting the input signal for error before decoding (specification, paragraph # 0027). As long as 'the evaluation of digital signal' is concerned, it is noted that it is not novel to replace the analog circuitry with digital. For instance, Weiss is teaching the digital signals being outputted after detecting the inputted signal for noise (responsible to generate an error) (figure 1, element 10, col.4, lines 23-43). Therefore, it is obvious to one ordinary skill in the art to implement the teaching of Weiss into Hachisuka in order to allow only the

wanted data to be retained or selected as taught by Weiss (col.2, lines 13-18) hence increase the system performance.

3. Applicant argues: "In summary, Hachisuka's switch 112 selects either a digital signal or an FM analog signal, in contrast to the "mode selector" recited in claim 1. In addition, the inverter 64 in the Weiss reference is used for disabling an amplifier so as to mute a speaker while a data signal is present. This is quite different from the "error generator" recited in claim 1". This is not persuasive. Weiss (secondary reference) is muting the unwanted data (claimed error data) and allowing the maximum amount of data to be retained (col.2, lines 13-18). Specifically, inverter 64 is being used to mute the amplifier until all the input signals to AND gate are high (col.3, lines 25-28). Therefore, Amplifier is not disabled all the time in order to mute the speaker, it is disabled only when the data is unwanted (it is noted that when the signal is unwanted (error data), amplifier is disabled in order to mute the specific path which carries this data and allow the other path to process (col.3, lines 16-33, col.4, lines 9-43). In other words, Weiss is selecting between data information signal and the digital signal that indicates the presence or absence of data with respect to unwanted signal by mute control signal 40 coupled with inverter 64 (figure 1) (col.3, lines 16-33 & 61-68, col.4, lines 1-43). Furthermore, although Hachisuka is not muting the signal but his teachings suggest that noise detecting circuit 109 may comprise a squelch circuit (col.4, lines 19-27) (which suppresses or mutes the noise well known in the art). It would have been obvious to one ordinary skill in the art to modify the Hachisuka's (primary reference) circuit with Weiss's (secondary reference) inverter 64 in order to indicate the unwanted

(error data) presence and decode the signal accordingly as taught by Weiss (col.2, lines 13-18) hence increase the system performance.

4. Applicant argues: "Claim 2 provides that the "mode selector" of claim 1 comprises first and second selectors. However, an ordinarily skilled person would have had no reason to think that Shinozaki's selectors 164 and 168 select "either of a reproduction mode of reproducing the digital signals or an evaluation mode of evaluating the digital signals" in accordance with claims 1 and 2 together". This is not persuasive. Claim 2 limitations of having reproduction mode and evaluation mode are being rejected with claim 1 on which claim 2 depends (see claim 1 rejection, Office Action 12/30/2005). Shinozaki reference is combined with other two references mentioned in claim 1 rejection in order to reject the claim 2 limitations of having two selectors (see claim 2 rejection, Office Action 12/30/2005).

5. Applicant argues: "Nor do Shinozaki's selectors 164 and 168 represent "a pair of signal pole, double throw switches that are connected to one another, both switches being responsive to a common selection signal". This is not persuasive. This is a new matter addition because Examiner does not find the description of the claim 19 limitations in the specification.

Response to Amendment

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 19 is rejected under 35 U.S.C. 112, first paragraph because the limitations in the claim is not disclosed in the specification and makes it difficult to understand the claim invention.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hachisuka et al. (5,598,430), hereinafter referred to as Hachisuka, in view of Weiss (5,151,922).

10. Refer to claim 1, Hachisuka teaches, demodulation of the signal (see col.1, lines 41-47), 'a mode selector (see figure 1, element 112) for selecting either of a reproduction mode of reproducing the digital signals (see figure 1, element 108, col.4, lines 14-16) and an evaluation mode of evaluating the digital signals' (see figure 1, elements 107, 109, & 110, col.4, lines 14-16) (it should be noted that in figure 1 switch 112 (claimed mode selector) is selecting between digital signal detecting circuit 108 (claimed 'reproduction mode') or the output from the digital signal detecting circuit 107 (claimed 'evaluation mode') according to the result of the determination by the logic discriminating circuit 111 (col.4, lines 38-48) which gets inputted by the noise detection circuit 109 and RSSI detecting circuit 110 (claimed error generator) since as it is

disclosed in the specification that reproduction mode is the mode which outputs the inputted digital value directly to ADPCM CODEC without going through the error detection stage of the circuit while evaluation mode is responsible to output the digital signal through error generator to error detector (Specification, page # 8, paragraph # 0026 & page # 9, paragraph # 0027) . Hachisuka is selecting one of the circuits (figure 1, elements 108 and 107) through (figure 1, element 112) and the process of detecting noise and strength of the received signal is included when element 112 selects circuit 107 (as described above) and therefore it is considered to be equivalent to applicant's limitations of having two modes with error generator included. Furthermore, Specification does not clarify the advantage of inverting the level of the digital signal for the evaluation mode).

Hachisuka does not teach the inverting level of digital signal.

Weiss discloses, a demodulated signal (see figure 1, ' DEMODULATED SIGNAL') and inverting the digital signal (see figure 1, element 64, col.3, lines 21-28).

It would have been obvious to one ordinary skill in the art to implement the teachings of Hachisuka into Weiss in order to disable the speaker while data signal is present (selecting one of the mode depending on what type of signal is present) as taught by Weiss (see col.3, lines 21-28).

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hachisuka et al. (5,598,430), hereinafter referred to as Hachisuka, and Weiss (5,151,922), as applied to claim 1 above, and further in view of Shinozaki et al. (US 6,687,512), hereinafter referred to as Shinozaki.

12. Refer to claim 2, Hachisuka and Weiss teach all the limitations in the previous claim on which claim 2 depends but they fail to disclose two selectors.

Shinozaki discloses, 'a first selector' (see figure 6, element 164, col.6, lines 4-18), and 'a second selector' (see figure 6, element 168, col.6, lines 4-18)).

It would have been obvious to one ordinary skill in the art to implement the teachings of Shinozaki into Hachisuka and Weiss in order to select a destination of digital signals and a source as to be able to switch to different modes based on the types of the signals inputted as taught by Shinozaki (see col.2, lines 15-19).

13. Claims 3, 4, 7, 8, 11, 12, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hachisuka et al. (5,598,430), hereinafter referred to as Hachisuka, Weiss (5,151,922) and Shinozaki et al. (US 6,687,512), hereinafter referred to as Shinozaki, as applied to claims 1 and 2 above, and further in view of Hori et al. (US 2003/0117926), hereinafter referred to as Hori.

14. Refer to claim 3, Hachisuka, Weiss, and Shinozaki teach all the limitations in the previous claims on which claim 3 depends but they fail to disclose 'a pulse outputting circuit'.

Hori discloses, 'a pulse outputting circuit for outputting pulse signals at the predetermined timing' (see figure 2, element 110, page # 3, paragraph # 0045 and 0047, and page # 4, paragraph # 0054) (Note: element 103 supplies pulse to element 110); and an inverter for inverting the level of the digital signals responsive to a transmission of the pulse signals (see figure 3, element 601, page # 3, paragraph # 0045 and 0046).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Hachisuka, Weiss and Shinozaki as to detect and set the value of an error signal as taught by Hori (see page # 5, paragraph # 0073).

15. Refer to claim 4, Hachisuka, Weiss, and Shinozaki teach all the limitations in the previous claims on which claim 4 depends but they fail to disclose 'a preset value holding circuit'.

Hori discloses, 'said error generator (see figure 2, element 107, page # 4, paragraph # 0052) comprises a preset value holding circuit (see figure 2, element 108, page # 4, col.1, paragraph # 0054) which has a preset value defining a transmission timing of the pulse signals set from outside said apparatus to hold the preset value to supply the preset value to said pulse outputting circuit (see figure 2, element 110, figure 3) and (page # 3, paragraph # 0046 and 0047).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Hachisuka, Weiss and Shinozaki in order to divide and synchronize and external clock or pulse as taught by Hori (see page # 1, col.2, paragraph # 0013, lines 45-49).

16. Refer to claim 7, Hachisuka, Weiss, and Shinozaki teach all the limitations in the previous claims on which claim 3 depends but they fail to disclose an error detector explicitly.

Hori discloses, 'an error detector (see figure 2, element 109A or 109B) interconnected to said mode selector for detecting an error contained in the digital signals (see figure 2, element 102); said error detector supplying said pulse outputting

circuit (see figure 2, element 110) with an output timing defining a field of the digital signal in which check data for received data are held' (see page # 3, col.2, paragraph # 0047).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Hachisuka, Weiss and Shinozaki in order to have signals in synchronization with pulse generator as taught by Hori (see page # 3, col.2, paragraph # 0049, lines 27-30).

17. Claim 8 is rejected under the same rational as claim 7 above.

18. Refer to claim 11, Hachisuka, Weiss, and Shinozaki teach all the limitations in the previous claims on which claim 11 depends but they fail to disclose 'a sync pattern detector'.

Hori discloses, 'a sync pattern detector interconnected to said mode selector for detecting a sync pattern contained in the digital signals (see figure 2, elements 102 and 105); said sync pattern detector supplying said pulse outputting circuit with an output timing defining a field of received data which follows the sync pattern and holds check data' (see figure 2, elements 102, 105, and 106, page # 3, col.2, paragraph # 0050 and page # 5, col.2, paragraph # 0070).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Hachisuka, Weiss, and Shinozaki as to detect the fix pattern and output a sync pattern detection as taught by Hori (see page # 2, col.1, paragraph # 0018, lines 17-20).

19. Claim 12 is rejected under the same rational as claim 11.

20. Refer to claim 16, Hachisuka, Weiss, and Shinozaki teaches all the limitations in the previous claims on which claim 16 depends but they fail to disclose an error detector and a time selector explicitly.

Hori discloses, 'an error detector for detecting an error contained in the digital signals (see figure 2, elements 109A, and 109B combined, page # 4, paragraph # 0053 and 0058); and a timing selector for selecting an output timing supplied from either of said error detector and said sync pattern detector' (see figure 2, element 106) and (page # 3, paragraph # 0049 and page # 4, paragraph # 0052).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Hachisuka, Weiss, and Shinozaki in order for a time selector to check if the inputted signal by error detector represents the presence or absence of error signal as taught by Hori (see page # 4, col.1, paragraph # 0052, lines 9-12) and if the inputted sync detection signal represents the absence or presence of the detection to timing generator as taught by Hori (see page # 3, paragraph # 0049, col.2, lines 27-46 and paragraph # 0050).

21. Claim 17 is rejected under the same rational as claim 16 above.

22. With respect to claim 19, Hachisuka discloses a switch 112 with two poles and one pole (figure 1) in order to make the selection between circuits 108 and 107 (figure 1). Switch 112 (figure 1) selects one of the circuits which has signals associated with them (claimed common selection signal) (col.4, lines 38-48) hence reads on claim limitations.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Retzer et al. (5, 465,404) disclose communications receiver with an adaptive squelch system.
- McDonough (5,778,024) teaches dual-mode communications processor.
- Sutphin et al. (4,663,765) disclose data muting method and apparatus for audio-digital communications systems.

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naheed Ejaz whose telephone number is 571-272-5947. The examiner can normally be reached on Monday - Friday 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Naheed Ejaz
Examiner
Art Unit 2611

N.E.
7/19/2006

Pankaj Kumar
Primary Examiner